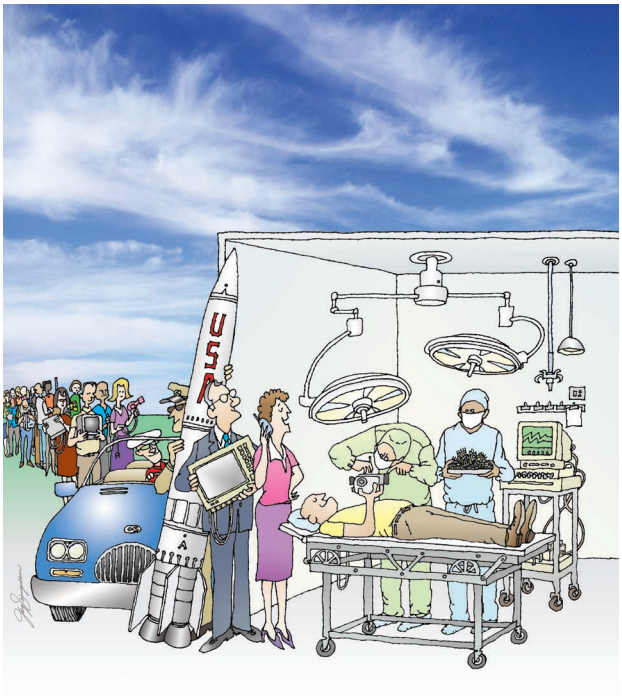

Guest Editors' Introduction

Opportunities and Challenges in Embedded Systems

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Embedded systems are most directly defined as computer systems embedded inside larger systems. But that does not capture the reason these systems have emerged as such active research and commercial targets. By their very nature of being located inside a myriad of systems, embedded systems span a wide range of system requirements. If there is one unifying characteristic, it is that the design goals are often wildly at odds. For example, most portable communication devices require supercomputer-class processing capabilities for audio, imaging, and video processing, but must run on a very limited battery power supply and fit in a pocket-friendly form. Compounding this are the often tight cost constraints and very aggressive time-to-market requirements. These conflicts are why embedded systems present such interesting research and commercial challenges.

The tight constraints force designers to tune and innovate at every level of the underlying computer system from processor microarchitecture, to the OS, to the application software. With tight time to market, they cannot design new systems from scratch and require ways to accelerate the design process. This leads to the reuse of multiple intellectual property modules in systems on chip (SoCs), a strategy that presents interesting challenges in system building. Selecting the right microarchitecture for the core processor is nontrivial. And compiling for these systems is significantly more complex than for general-purpose computing. This issue of *IEEE Micro* covers these challenges with articles on diverse aspects of embedded systems.

Many embedded systems execute real-time code and have complex hardware accelerators attached. The real-time software often has gaps or holes in its schedule that a programmer can exploit to reimplement the complex hardware accelerators in software. But the gaps are often too fine-grained for a simple, dynamic, process-context-switching solution. In his article, Dean explains how to merge two or more threads together at compile time to enable simpler hardware via the hardware-to-software migration of complex accelerators.

To deal with real time constraints, current embedded processors are often in-order

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processors, ensuring that the execution times of applications are predictable. As embedded processors become more complex, simultaneous multithreaded (SMT) processors become viable because of their good cost-performance tradeoff. However, there is a problem: SMT performance is too unpredictable to support real-time tasks. The article by Cazorla et al. presents a solution using a novel collaboration between the operating system and SMT.

Cache coherence is a classic problem in multiprocessor computer architecture, but the heterogeneous processing typically employed in SoC embedded applications provides new challenges. Suh, Lee, and Blough present a hardware-software methodology to maintain cache coherency in a heterogeneous platform. The goal is to help embedded-systems programmers, usually not expert in concurrent programming, with a transparent view of shared data, thus avoiding explicit software synchronization.

Nowadays, designers can develop inexpensive and specialized SoC solutions using hybrid chips containing both CPU and FPGA components. The exploitation of their full potential presents an interesting challenge for system developers, who could also try to apply reuse best practices that reduce cost and time to market. Andrews et al. discuss these topics, underscoring the need for defining a new hybrid computational model in this context.

Design space exploration is one of the most important activities in producing a successful product. Finding the best tradeoff among conflicting requirements is highly complex. Stream processors illustrate this complexity. Digital signal processors (DSPs) targeted toward high-performance embedded applications, stream processors contain clusters of functional units and provide a bandwidth hierarchy, often supporting hundreds of arithmetic units in a single processor. Rajagopal, Cavallaro, and Rixner present a tool that explores the design space of candidate stream processor configurations, taking into account estimates of power consumption and real-time performance.

In their article, Krall et al. focus on the role of compilers within the design process and describe their experience in the DSP field. Their basic idea is to introduce a hardware feature only when an application can leverage it through an optimizing compiler, obtaining a very convenient programmability-to-performance ratio. The presented experimental results show the actual possibility of also using high-level languages like C++ to take full advantage of all the DSP features.

Taken as a whole, the articles in this special issue illustrate the active topics in both industrial embedded-system development and in the research of new and better embedded-system designs. MICRO

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